AMENDMENTS TO THE CLAIMS

Claims 1-12 (cancelled)

Claim 13 (currently amended): A method for manufacturing a heat dissipating power amplifier integrated circuit, the method comprising:

providing a substrate;

providing a heat sink for dissipating heat;

integrally forming a transistor on the substrate, the transistor comprising a collector, a base, and at least an emitter <u>including an enlarged portion located laterally away from the collector and the base</u>; and

directly connecting the heat sink and the emitter using an emitter electrode.

Claim 14 (original): The method of claim 13 wherein forming the transistor comprises:

disposing a metallization layer on the substrate to form the emitter; and

disposing a second metallization layer to mutually connect emitters.

Claim 15 (original): The method of claim 13 further comprising:

electrically grounding the emitter through the emitter electrode and the heat sink.

Claim 16 (original): The method of claim 13 further comprising:

arraying a plurality of transistors and a plurality of emitter electrodes to form a functional device.

Claim 17-20 (cancell d)

Claim 21 (previously presented): A power amplifier integrated circuit comprising:

a substrate;

a transistor disposed on the substrate, the transistor including a collector, a base, and an emitter, the emitter including an enlarged portion located laterally away from the collector and the base;

a heat sink for dissipating heat; and

a flip-chip bump connecting the heat sink and the enlarged portion of the emitter.

Claim 22 (previously presented): The power amplifier integrated circuit of claim 21 wherein the flip-chip bump and the heat sink provide an electrical ground connection to the emitter.

Claim 23 (previously presented): A power amplifier integrated circuit comprising:

a substrate;

a transistor disposed on the substrate, the transistor including a collector, a base, and an emitter, the emitter including an enlarged portion located laterally away from the collector and the base;

a heat sink for dissipating heat; and

a via connecting the heat sink and the enlarged portion of the emitter, the via penetrating the substrate at the location of the enlarged portion of the emitter.

Claim 24 (previously presented): The power amplifier

integrated circuit of claim 23 wherein the via and the heat sink provide an electrical ground connection to the emitter.

Claim 25 (previously presented): The power amplifier integrated circuit of claim 21 wherein the transistor is integrally formed on the substrate.

Claim 26 (previously presented): The power amplifier integrated circuit of claim 23 wherein the transistor is integrally formed on the substrate.

Claim 27 (new): A power amplifier integrated circuit comprising:

a planar substrate;

a transistor integrally formed on the substrate, the transistor including a collector, a base, and an emitter, the emitter including an enlarged portion;

a heat sink for dissipating heat; and

an emitter electrode directly electrically and thermally connecting the heat sink and the enlarged portion of the emitter;

wherein in the plane of the substrate, the area of the enlarged portion of the emitter is greater than the area of the emitter electrode, and the enlarged portion of the emitter has a center of area located laterally away from the collector and the base by at least half a major dimension of the emitter electrode.

Claim 28 (new): The power amplifier integrated circuit of claim 27 wherein the transistor is a heterojunction bipolar

transistor (HBT).

Claim 29 (new): The power amplifier integrated circuit of claim 27 wherein the emitter comprises a metallization layer.

Claim 30 (new): The power amplifier integrated circuit of claim 27 wherein the emitter electrode is a flip-chip bump.

Claim 31 (new): The power amplifier integrated circuit of claim 30 wherein the heat sink and the substrate sandwich the transistor.

Claim 32 (new): The power amplifier integrated circuit of claim 27 wherein the emitter electrode is a backside via penetrating the substrate.

Claim 33 (new): The power amplifier integrated circuit of claim 32 wherein the heat sink and the transistor sandwich the substrate.

Claim 34 (new): The power amplifier integrated circuit of claim 27 comprising more than one emitter, and emitters are mutually connected by a metallization layer.

Claim 35 (new): The power amplifier integrated circuit of claim 27 wherein the emitter electrode and the heat sink provide an electrical ground connection to the emitter.

Claim 36 (new): The power amplifier integrated circuit of claim 27 wherein the heat sink is a metal layer.

Claim 37 (new): The power amplifier integrated circuit of claim

27 wher in a plurality of transistors and a plurality of emitter electrodes are disposed in an array, and operate as a functional device.

Claim 38 (new): The power amplifier integrated circuit of claim 27 wherein the substrate is a GaAs substrate.